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HITA ★ U11 U14 91-370649/51 ★EP-461-639-A

Plastic-moulded-type semiconductor device - includes two large chips with surface electrodes mounted facing each other to form thin package

HITACHI KK 15.06.90-JP-155167

(18.12.91) H01l-23/49 H01l-25/06

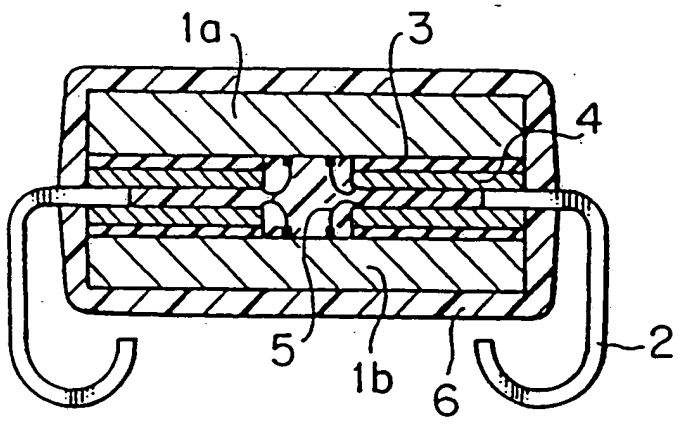
12.06.91 as 109654 (1550DM) - (E) No-SR.Pub R(DE FR GB IT)

The plastic-molded device comprises: two chips (1a, 1b) with surface electrodes (7) and circuits facing each other; lead frame (2) between the chips and insulation (3) on the main surfaces except for the electrodes and on which wiring patterns are formed which are connected to the electrodes and lead frame. A plastic package (6) sealing the chips, lead frame, insulation and wiring pattern.

Connections (5) between wiring pattern and chips, and parts of the chip surfaces not covered with insulation, are selaed with a first resin which is sealed by the plastic package. Wiring patterns are connected to the lead frame by soldering or by a conductive resin. The chips are rectangular and the electrodes are arranged along a centre line. The chips are memory LSIs and the wiring pattern are metallic foils.

ADVANTAGE - Two chips whose electrodes are in middle sections can be encased in single package. (19pp Dwg.No.2/20)

N91-283773 **U11-D1A3 U11-D3D U14-A20**



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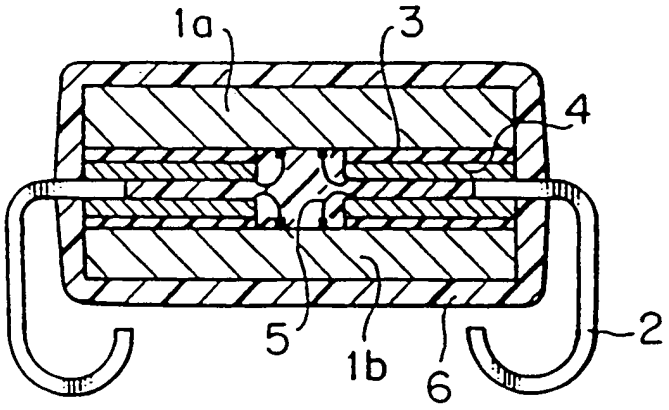

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 461 639 A2**

(12) EUROPEAN PATENT APPLICATION

(21) Application number: **91109654.3**

(22) Date of filing: **12.06.91**

(51) Int. Cl.5: **H01L 23/495**, H01L 23/498, H01L 25/065, H01L 23/31

(30) Priority: **15.06.90 JP 155167/90**

(43) Date of publication of application: **18.12.91 Bulletin 91/51**

(84) Designated Contracting States: **DE FR GB IT**

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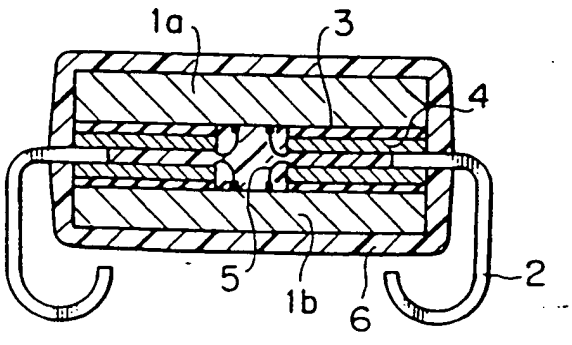
(54) Plastic-molded-type semiconductor device.

(57) A plastic-molded-type semiconductor device comprises two semiconductor chips (1a, 1b) having main surfaces on which electrodes and circuits are formed and which face each other; a lead frame (2) placed between these two semiconductor chips (1a, 1b) and electrically connected to their electrodes; a plastic package (6) formed by plastic-sealing the above components; and wiring patterns (4) provided on the main surfaces of the semiconductor chips (1a, 1b) through the intermediation of insulating films (3). The wiring patterns (4) are electrically connected to the electrodes of the semiconductor chips (1a, 1b) and to the lead frame (2). With this structure, it is possible for two large-sized semiconductor chips (1a, 1b) having electrodes in their middle sections to be encased in a single, relatively thin package (6).

FIG. 2



EP 0 461 639 A2

the chips having a wiring pattern face each other, with a lead frame being placed therebetween.

Subsequently, the wiring patterns are electrically connected to the lead frame by soldering or the like.

Finally, the two semiconductor chips and that part of the lead frame positioned between the chips are plastic-molded, and then the outer leads of the lead frame are shaped appropriately.

In the package of the present invention, a wiring pattern with an arbitrarily designed configuration is used, so that electrodes of the chips and the lead frame can be electrically connected to each other at arbitrary positions. Thus, even when two chips having electrodes arranged near the chips' center lines are used, as is the case with a LOC package, they can be encased in a single package.

Further, since there are no electrically connecting members between the side surfaces of the chips and those of the package, the chips may extend up to the vicinity of the external contour of the package, thus attaining a higher level of integration.

The increase in thiskness as a result of adopting the encasement process of this invention as compared to conventional single-chip packaging is basically no more than that attributable to the thickness of the additional chip itself. Thus, this invention is advantageous with respect to packaging making less thickness as that for encasing two chips.

Further, since it allows direct application of conventional techniques, such as the manufacturing technique for LOC packages and the tape-automated bonding technique, this kind of packaging is suitable for mass production.

Constructed as described above, the present invention provides the following advantages:

Due to the fact that the wiring pattern is provided on the semiconductor chip, two chips whose electrodes are in the middle sections thereof can be encased in a single package;

Since there is no need to provide electrically connecting members between the side surfaces of the chip and those of the package, chips of a larger size can be encased; and

The thickness of the plastic-molded-type semiconductor device of this invention can be as small as 1.1 mm.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a partially cutaway perspective view of a plastic-molded-type semiconductor device in accordance with a first embodiment of the present invention;

Fig. 2 is a sectional view of the same;

Fig. 3 is an enlarged sectional view showing a portion around electrodes of this plastic-molded-type semiconductor device;

Fig. 4 is an enlarged sectional view showing a portion around a side surface of the package of this plastic-molded-type semiconductor device;

Fig. 5 is a diagram illustrating a method of producing the plastic-molded-type semiconductor device of the first embodiment;

Figs. 6 through 11 are sectional views showing plastic-molded-type semiconductor devices which are partial modifications of the first embodiment;

Fig. 12 is an enlarged sectional view showing a part of a plastic-molded-type semiconductor device in accordance with a second embodiment of this invention;

Fig. 13 is an enlarged sectional view showing a part of a partial modification of the plastic-molded-type semiconductor device of the second embodiment;

Fig. 14 is an enlarged sectional view showing a part of a plastic-molded-type semiconductor device in accordance with a third embodiment of this invention;

Fig. 15 is an enlarged sectional view showing a part of a plastic-molded-type semiconductor device in accordance with a fourth embodiment of this invention;

Fig. 16 is an enlarged sectional view showing a part of a plastic-molded-type semiconductor device in accordance with a fifth embodiment of this invention;

Fig. 17 is a perspective view showing the internal structure of a conventional lead-on-chip package;

Fig. 18 is a plan view showing a layout of an optimum design for a 64 Mbit DRAM; and

Figs. 19 and 20 are illustrations of the electrical connection between electrodes of the chip and inner leads.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Embodiments of the present invention will now be described with reference to the accompanying

The first resin 10a and 10b may be of the same kind as a second resin plastic encapsulant 6, which is used for the encapsulating of the entire unit. Alternatively, it may be a soft resin such as silicon gel. In any case, the first resin used must have a satisfactory adhesiveness with respect to those surfaces of the semiconductor chips 1a and 1b on which circuits are formed.

Fig. 14 is a sectional view showing a part of a plastic-molded-type semiconductor device in accordance with the third embodiment of the present invention. In this embodiment, the adhesive layers 8c and 8d also serve as the insulating films, which means the insulating films 3 can be omitted. Thus, due to this arrangement, the thickness of the package can be reduced by double the thickness of the insulating film 3. In this embodiment, the electrical insulation between the circuits on the semiconductor chips 1a and 1b and the wiring patterns is ensured, so that the arrangement of this embodiment is particularly effective in a case where a protective film of polyimide or the like is formed on the surfaces of the chips.

Fig. 15 is a sectional view showing a part of a plastic-molded-type semiconductor device in accordance with the fourth embodiment of the present invention. In this embodiment, metallic foils 11 are employed as the wiring patterns, so that the package can have a relatively reduced thickness. It is difficult to attach patterned metallic foils to the insulating films 3, so, instead of doing this, the patterning of the metallic foils may be effectively performed by etching after attaching the foils to the films, as is practiced in the tape-automated bonding technique. After attaching the films, which have thus been patterned in this embodiment, to the chips 1a and 1b, the plastic-molded-type semiconductor device of this embodiment can be produced according to the procedures following the steps (404) shown in Fig. 5. Copper is an example of the material which can be used for the metallic foils.

Fig. 16 is a sectional view showing a part of a plastic-molded-type semiconductor device in accordance with the fifth embodiment of the present invention. In this embodiment, metallic foils 12 are used as the wiring patterns. In the vicinity of the device electrodes 7, certain portions 13 of these metallic foils 12 extend beyond the insulating films 3, and these portions 13 are electrically connected to the electrodes 7 by thermocompression bonding through the intermediation of solder, gold-silicon eutectic alloy, etc. In this package structure, no wires are needed, so that there is no need to secure the dimension corresponding to the height of the wires, thus making it possible to further reduce the thickness of the package as compared to the fourth embodiment. An estimated package thickness in this embodiment when using the present packaging technique is as small as 1.1 mm. The connection between the metallic foils 13 and the electrodes 7 can be easily effected by adopting the tape-automated bonding technique.

The above embodiments of this invention can be adequately applied to memory ICs. In particular, they can be very effectively applied to a 64 Mbit DRAM, which has the highest degree of integration at present. It will be described in the following how the first embodiment of the present invention can be applied to a 64 Mbit DRAM.

As shown in Figs. 1 and 2, DRAM chips 1a, 1b are sealed in a SOJ (Small Out-line J-bend) type plastic-molding package.

The DRAM has a large capacity of 64 Mbits x 1 bit and is sealed in a plastic-molding type package of 300 mil x 850 mil.

Further, as shown in Fig. 18 (a plan view showing an optimum design layout for the DRAM 1), the DRAM 1 is formed on a wafer by an optimum design and divided into two 32 Mbit DRAM sub-chips 1a and 1b by a scribe area 1C. Each of the DRAM sub-chips 1a and 1b has four I/O buffer circuits (eight I/Os). By combining these I/O buffer circuits, eight I/O circuits are formed (sixteen I/Os). Further, with the arrangement of the eight I/O buffer circuits in each of the DRAM sub-chips 1a and 1b, up to x 1 bit, x 4 bits, x 8 bits, and x 16 bits, can be realized through recombination of the wiring.

Arranged on those surfaces of the DRAM sub-chips on which circuits are formed (hereinafter referred to as the "main surfaces") are memory cell arrays and peripheral circuits. In the memory cell array, which is described in detail below, a plurality of memory cells each storing 1-bit of information are arranged in a matrix-like manner. The peripheral circuits consist of direct peripheral circuits and indirect peripheral circuits. The direct peripheral circuit is a circuit which directly controls the writing and reading of information to and from the memory cells. The direct peripheral circuit includes a row address decoder circuit, a column address decoder circuit, a sense amplifier circuit, etc. The indirect peripheral circuit is a circuit which indirectly controls the operation of the direct peripheral circuit. It includes a clock signal generation circuit, a buffer circuit, etc.

The layout shown in Fig. 18 includes address buffer circuits ①, clock circuits ②, main amplifier circuits ③, input/output (I/O) buffer circuits ④, Vbb generation circuits ⑤, word voltage generation circuits ⑥, column decoders ⑦, row decoders ⑧, sense amplifier circuits ⑨, and memory arrays (512 Kbit arrays) ⑩, the reference symbol IBP indicates bonding pads.

Examples of optimum designs will be described in the following:

64 Mbit DRAM using four 16 Mbit DRAMs

Number of simultaneous operation bits:	8 kbits
Number of times of refreshment:	8192 times
Refreshment addresses:	13 addresses
Test mode	32 bits read simultaneously

Since the power consumption of a DRAM increases as the number of operation bits is augmented, the DRAM of the design (1) consumes more power than that of the design (2). Further, in the case of the design (1), the refreshment addresses are different from those in an ordinary DRAM, that is, this type of design lacks compatibility with ordinary DRAMs. In view of these problems, the present invention is concerned with the design (2).

Inner leads 2a are arranged on the respective main surfaces of the DRAM sub-chips 1a and 1b, i.e., on those surfaces on which the memory arrays ⑲ and peripheral circuits are arranged. Provided between these inner leads 2a and the DRAM sub-chips 1a and 1b are insulating films 3, which may consist, for example, of polyimide-type resin films. Adhesive layers (not shown) are provided on the surfaces of these insulating films 3, both on the side of the DRAM sub-chips 1a and 1b and on the side of the inner leads 2a. The material used for these adhesive layers may, for example, be a polyether-amide/imide-type resin or an epoxy-type resin.

As shown in Fig. 18, bonding pads (external terminals) IBP are provided in the center line sections in the longitudinal direction (the Y-direction) of the main surfaces of the DRAM sub-chips 1a and 1b. As shown in Fig. 19, on the DRAM sub-chip 1a, the electrical connection between these bonding pads IBP and the inner leads 2a is effected according to the normal arrangement by wire bonding through bonding wires 5. And, as shown in Fig. 20, on the DRAM sub-chip 1b, the electrical connection between the bonding pads IBP and the inner leads 2a is effected in a manner reverse to the normal arrangement by wire bonding through bonding wires 5.

Further, as shown in Fig. 2, the DRAM sub-chips 1a and 1b are layered one on top of the other in such a manner that each of the leads of one DRAM sub-chip has the same function as that lead of the other DRAM sub-chip to which it is connected.

This plastic-molding-type package 14 employs a LOC (Lead On Chip) structure in which inner leads 2a are arranged on both of the DRAM sub-chips 1a and 1b. In this plastic-molding-type package 14, which has the LOC structure, the inner leads 2a can be freely arranged without being restricted by the configuration of the DRAM sub-chips 1a and 1b. As a result, DRAM 1 having a larger size can be packaged. In other words, with this plastic-molding-type package 14, the package size can be relatively small even when DRAMs 1 of a still larger size are used with a view to meeting the demand for a larger capacity. Thus, with this package structure, an improvement can be attained in terms of packaging density.

One end of each inner lead 2a is integrally formed with one of outer leads. Each outer lead is standardized and numbered, with the signal to be applied thereto being specified. In Figs. 19 and 20, the reference numerals I/O0 to I/O7 indicate input terminals, A0 to A12 indicate address terminals, and the reference symbol Vcc indicates power voltage (Vcc) terminals. The power voltage Vcc may, for example, be an operation circuit voltage of 5V. The reference symbol WE indicates write enable signal terminals, RAS indicates row address strobe signal terminals, and Vss indicates reference voltage (Vss) terminals. The reference voltage Vss may, for example, be a circuit reference voltage of 0V. The reference symbols OE, CAS, and NC respectively indicate output enable signal terminals, column address strobe signal terminals, and dead terminals.

The other end section of each inner lead 2a extends across the respective longer sides of the rectangular DRAM sub-chips 1a and 1b to the central sections of these DRAM sub-chips. The tip of each of these other end sections of the inner leads 2a is connected through a bonding wire 5 to a bonding pad (an external terminal) IBP arranged in the central section of the DRAM sub-chip 1a. The bonding wires 5 consist of aluminum (Al) wires. Alternatively, the bonding wires 5 may also consist of gold (Au) wires, copper (Cu) wires, metal wires coated with an insulating resin, etc. The bonding with the bonding wires 5 is effected by the bonding method in which thermocompression bonding and ultrasonic oscillation are utilized.

lead frame (2) consisting of a set of leads and placed between said two semiconductor chips (1a, 1b), insulating films (3) which are provided on at least a part of the main surfaces of said semiconductor chips (1a, 1b) except for said electrodes (7) and on which metallic wiring patterns (4) are formed; said wiring patterns (4) being electrically connected to said electrodes (7) and said lead frame (2); and a plastic package (6) formed by plastic-sealing a part of said lead frame (2), said semiconductor chips (1a, 1b), said insulating films (3) and said wiring pattern (4).

2. The device of claim 1, wherein connecting portions (5) electrically connected said wiring pattern (4) to said semiconductor chips (1a, 1b) and those portions of the main surfaces of said semiconductor chips which are not covered with said insulating films (3) are at least partially sealed with a first resin (10a, 10b), and wherein said plastic package seals said first resin (10a, 10b) with a second resin (6).

3. The device of claim 1 or 2, wherein said electrodes (7) are electrically connected to said wiring patterns (4) through wires (5).

4. The device of claim 1 or 2, wherein certain metal portions (13) of said metallic wiring patterns (12) extend beyond said insulating films (3) and are electrically connected to said electrodes (7) by thermocompression bonding.

5. The device of any of claims 1 to 4, wherein said wiring patterns (4) are electrically connected to said lead frame (2) by soldering.

6. The device of claim 5, wherein the melting point of the solder used in the soldering is not lower than 250 °C.

7. The device of any of claims 1 to 4, wherein said wiring patterns (4) are electrically connected to said lead frame (2) by means of an electrical conductive resin (9).

8. The device of any of claims 1 to 7, wherein said semiconductor chips (1a, 1b) have a rectangular configuration, and wherein said electrodes (7) are arranged in the vicinity of at least one of the two center lines of the respective semiconductor chip (1a, 1b).

9. The device of any of claims 1 to 8, wherein said semiconductor chips (1a, 1b) are memory LSIs.

10. The device of any of claims 1 to 9, wherein said wiring patterns (12) are metallic foils.

FIG. 1

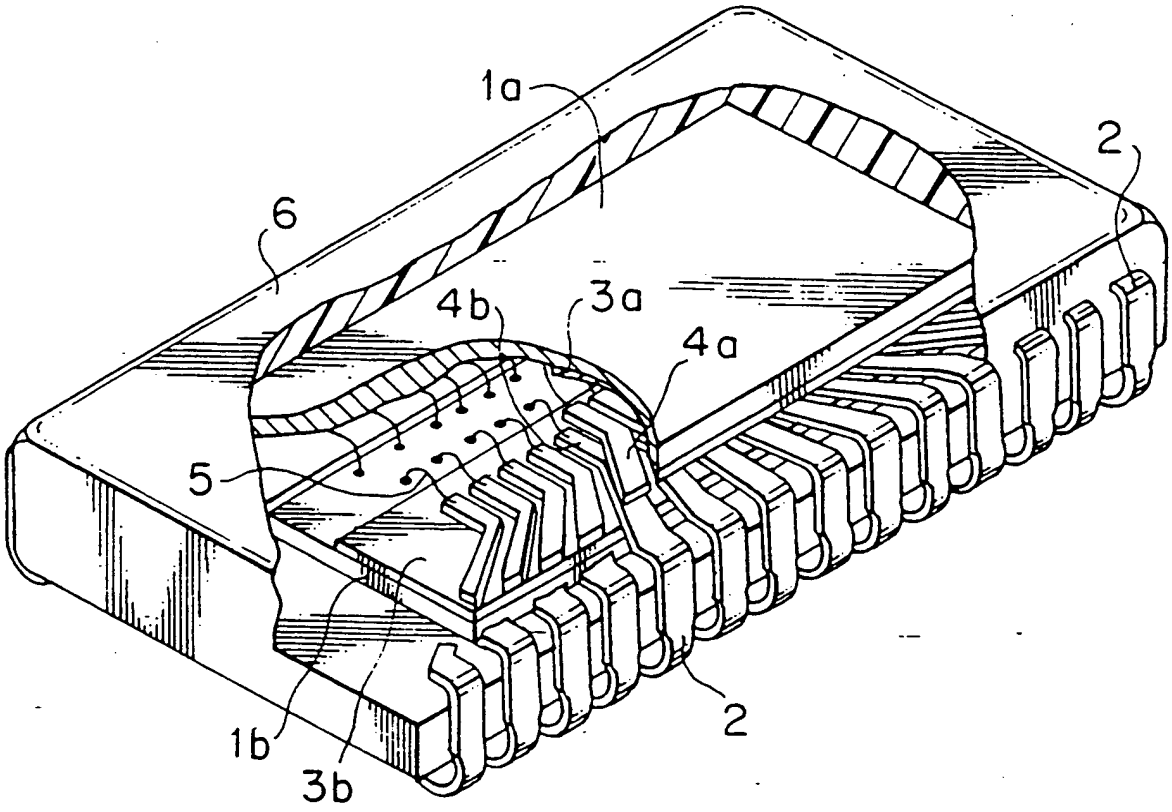


FIG. 2

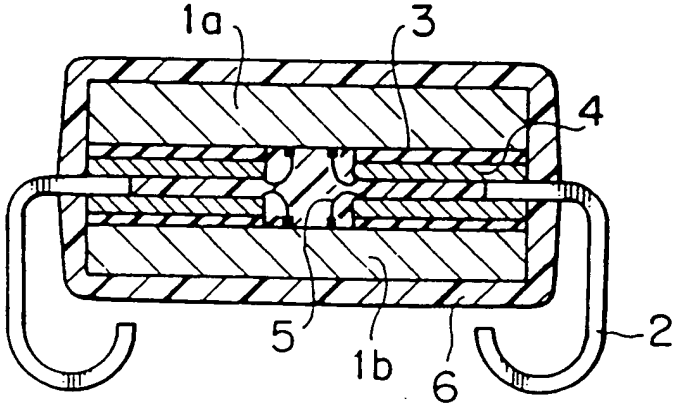


FIG. 3

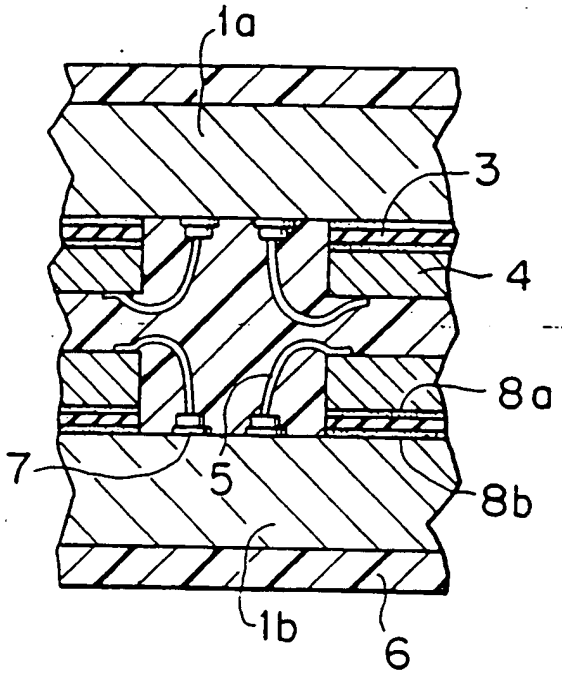


FIG. 4

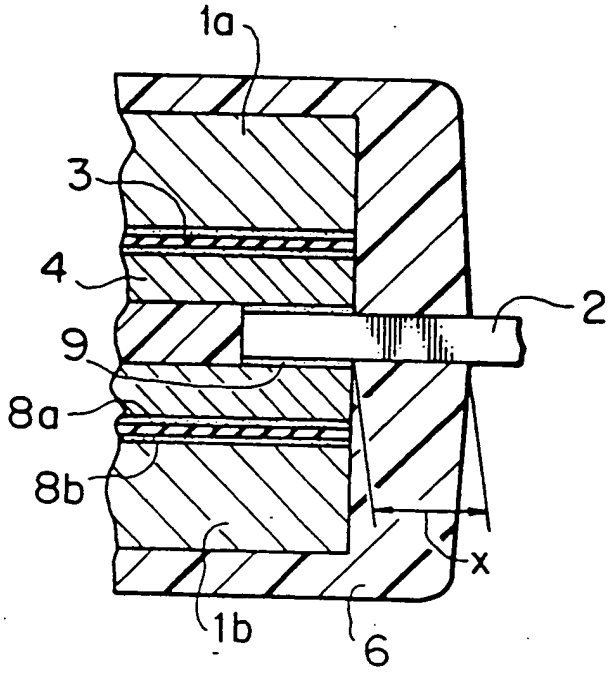


FIG. 5

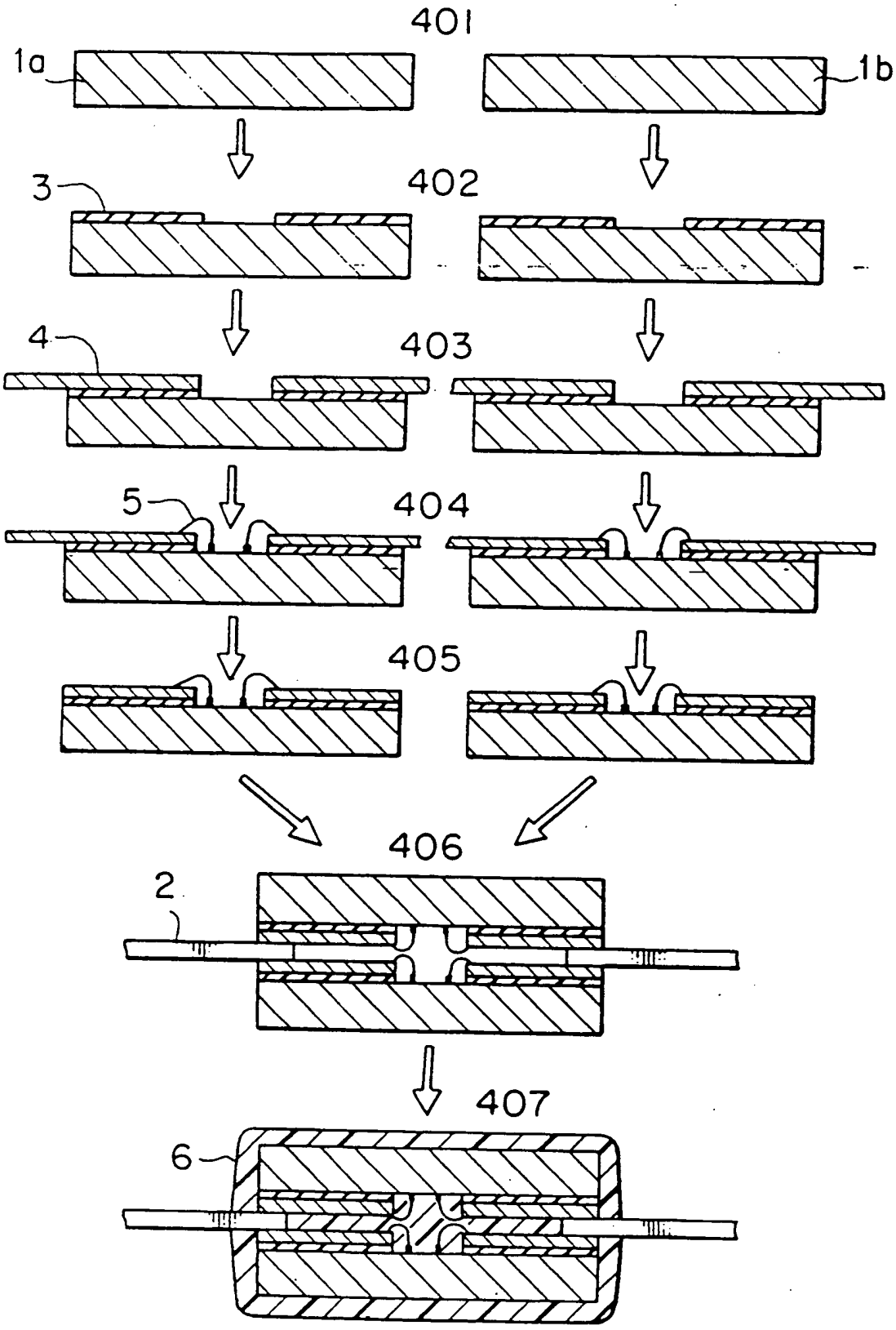


FIG. 6

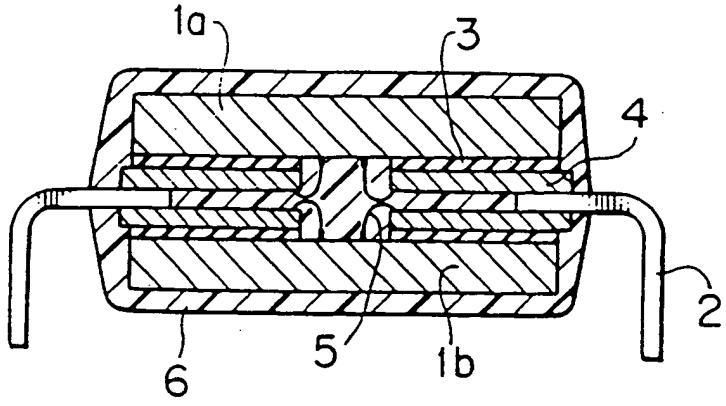


FIG. 7

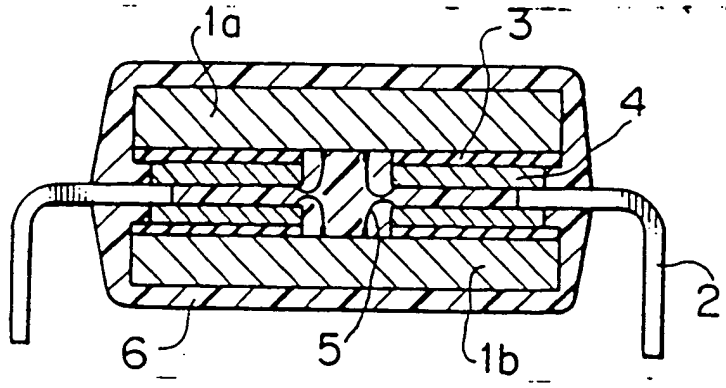


FIG. 8

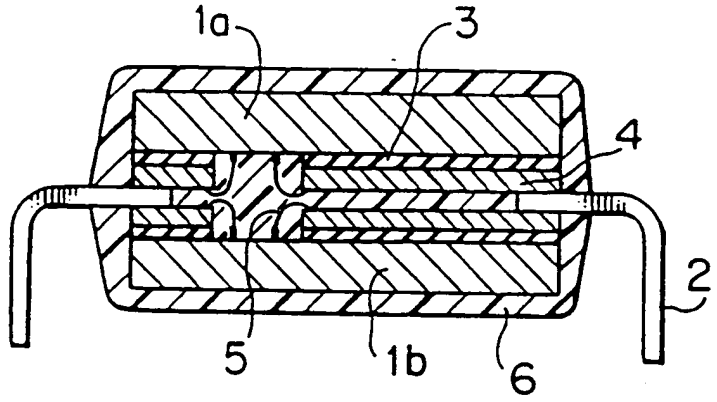


FIG. 9

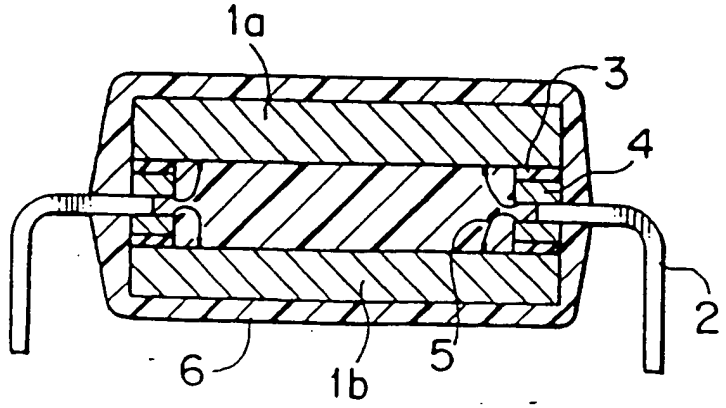


FIG. 10

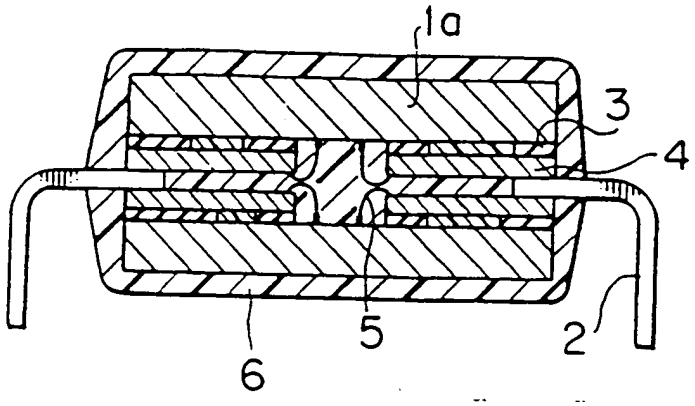


FIG. 11

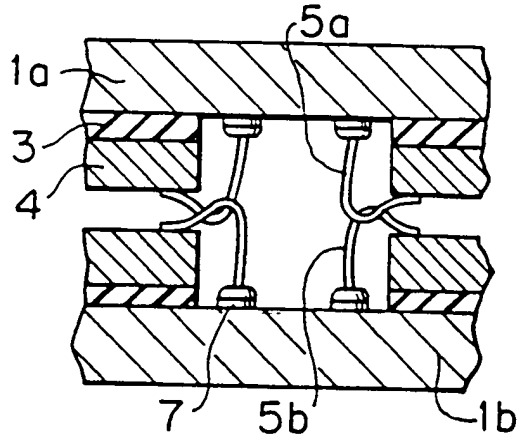


FIG. 12

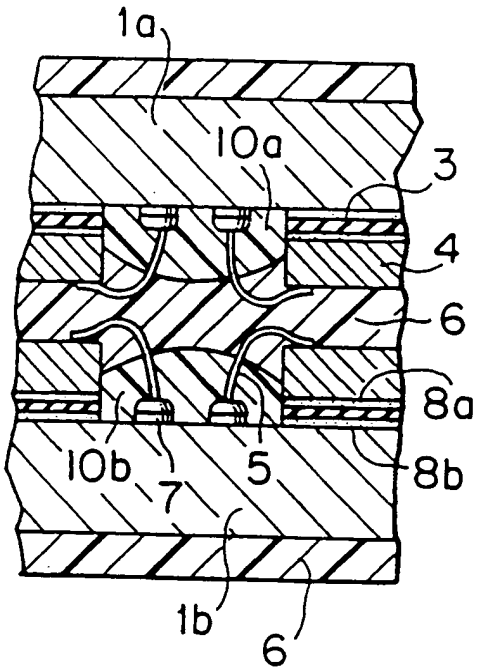


FIG. 13

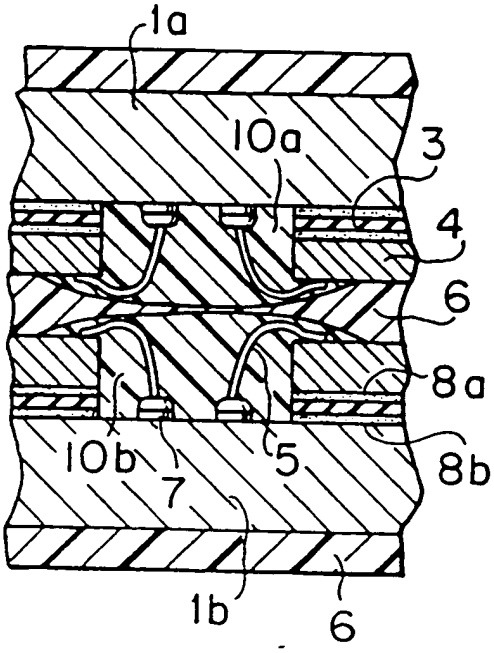


FIG. 14

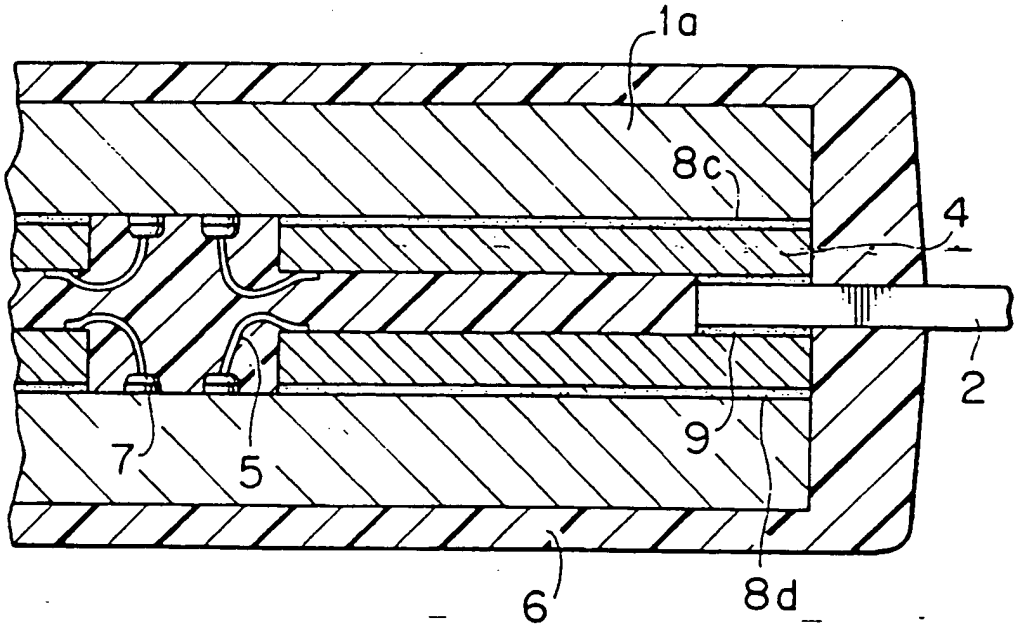


FIG. 15

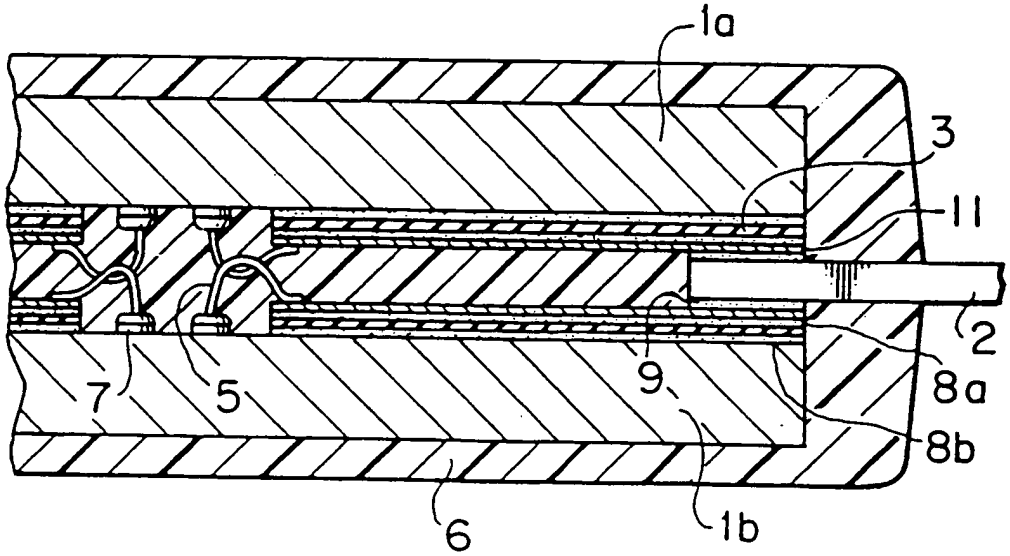


FIG. 16

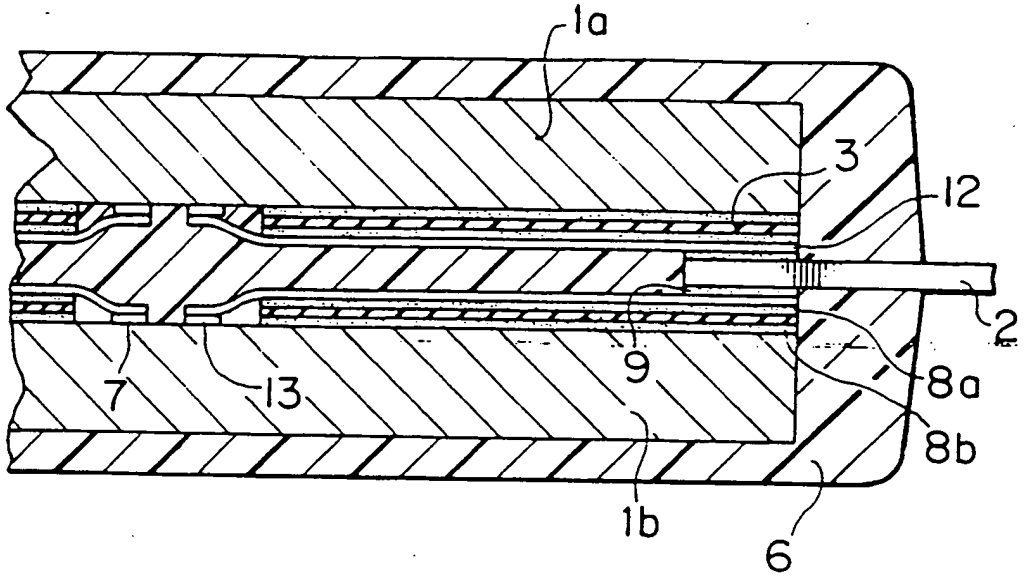


FIG. 17

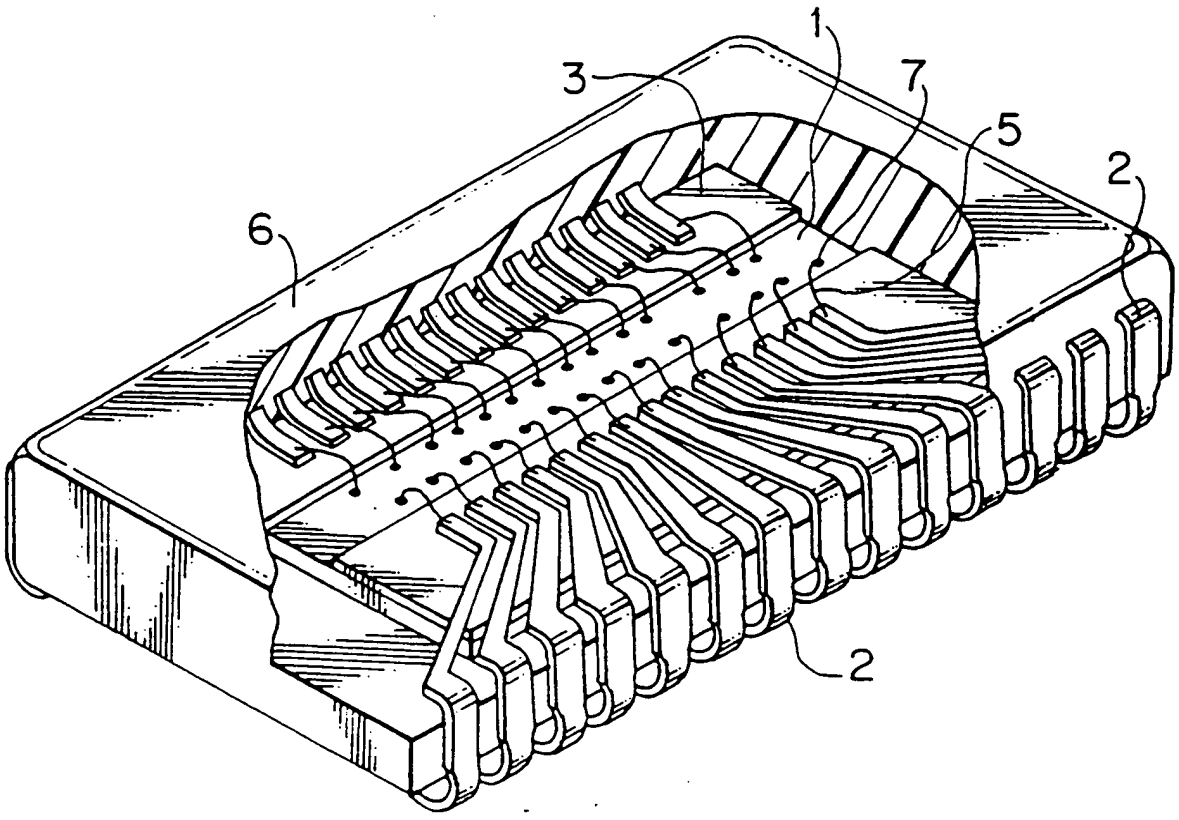


FIG. 18

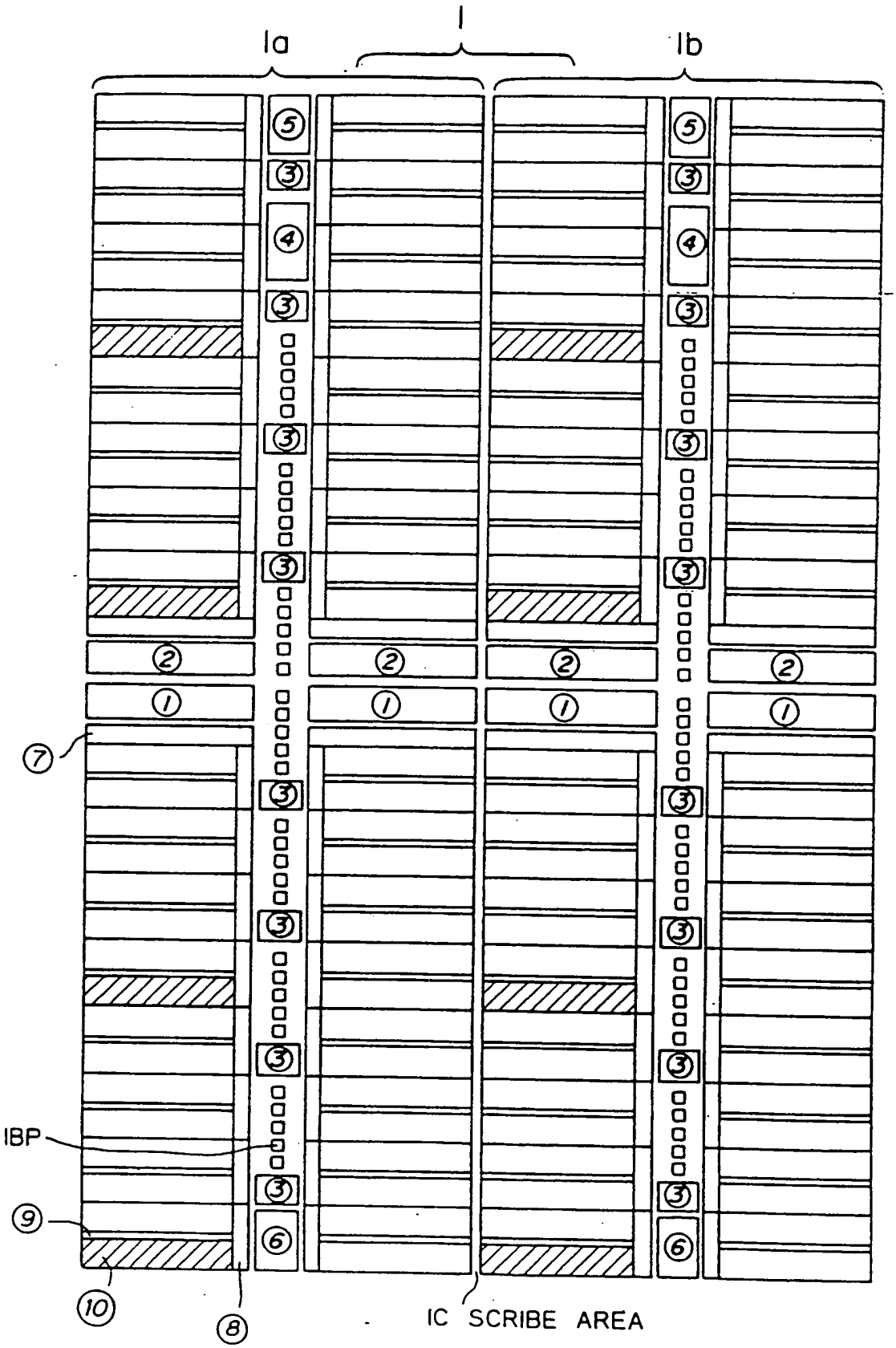
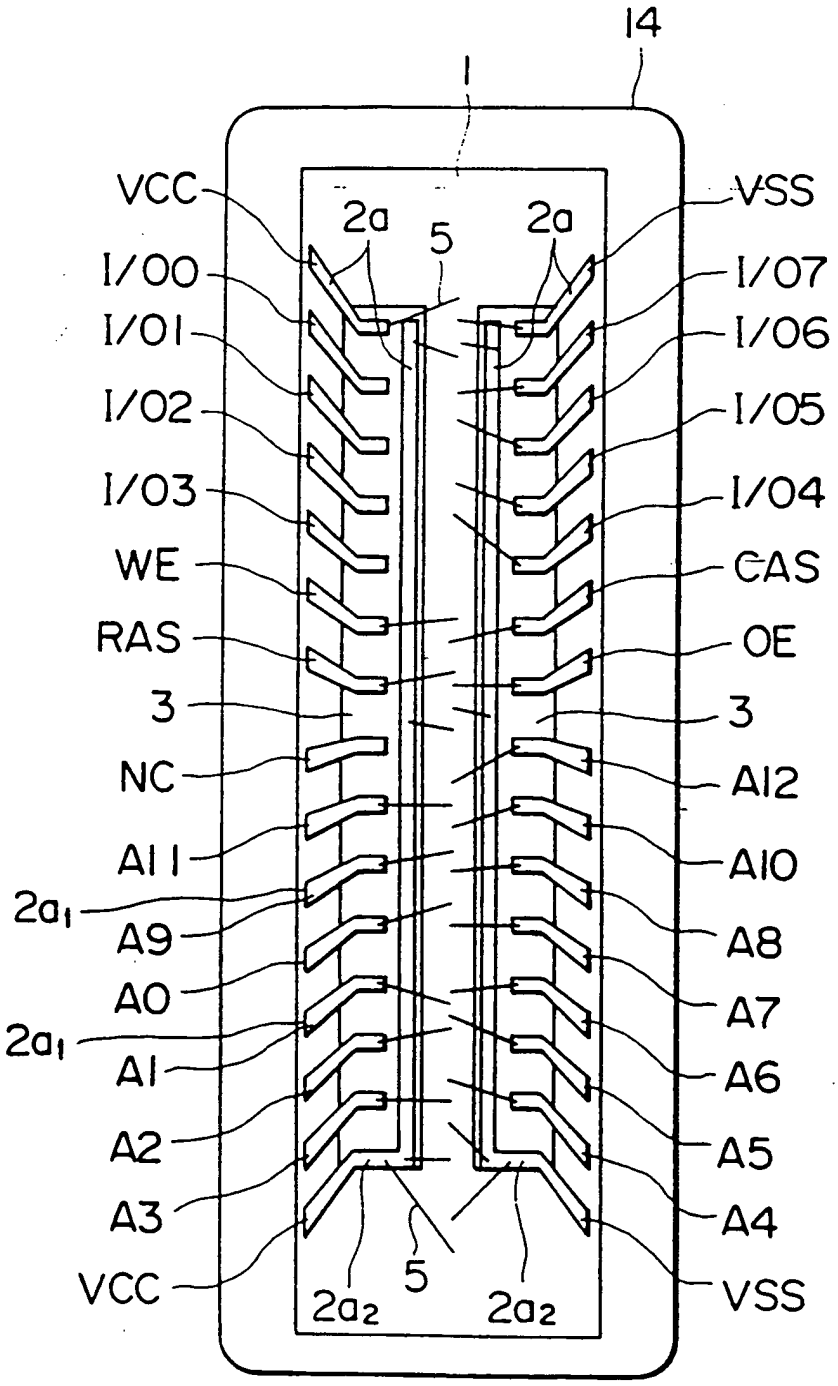


FIG. 19


14
1
VCC
I/O0
I/O1
I/O2
I/O3
WE
RAS
3
NC
A11
2a1
A9
A0
2a1
A1
A2
A3
VCC
2a
5
2a
VSS
I/O7
I/O6
I/O5
I/O4
CAS
OE
3
A12
A10
A8
A7
A6
A5
A4
VSS
5
2a2
2a2